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EXAMINER	
NGUYEN, LINH M	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 12/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,080	CAMPBELL, BRIAN J.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *07/10/03* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This is a reply to the Applicant's filing on 07/10/03 and preliminary amendment submitted on the same day. According to the information provided therein, original claims 1-20 are cancelled; claims 21-42 are newly added; and thus claims 21-42 are now presented in the instant application.

Claim Objections/Minor Informalities

1. Claims 22 and 36 are objected to because of the following informalities:

Claim 22, line 3, change "if" to -- when--;

Claim 36, line 3, change "if" to -- when--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 29-30, 33-34, and 40-41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claims 29-30, 33-34, and 40-41, the term "about" recited in lines 2 of the claims renders the claims indefinite as it does not indicate a positive determination of the size of the delay of (a) the second phase *(as recited in claims 29, 33 and 40)* or that of (b) 2 gate delays *(as recited in claims 30, 34 and 41)*. Defining the range(s) of delay specifically in the claims is suggested. Clarification is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 21-34 and 42 are rejected under 35 U.S.C. 102(a) as being anticipated by Weiss et al. (IEEE International Solid-State Circuits Conference, ISSCC 2002, February 2002, pp. 112-113).

With respect to claim 21, Weiss et al. discloses, in Fig. 6.7.2, a conditional clock buffer circuit having a clock output *(output from inverter which is input of latch circuit)* and coupled to receive a clock input *(half-frequency clock)* and a condition signal *(output from NOR gate)*, the conditional clock buffer circuit comprising 1) a first circuit *(first P-transistor connected to clock)* coupled to receive the clock input and coupled to a first node within the conditional clock buffer circuit, the first circuit configured to generate a first state on the first node responsive to a first phase of the clock input; 2) a second circuit *including the three N transistors)* coupled to receive the clock input and the condition signal and coupled to the first node, wherein the second circuit is configured to conditionally generate a second state on the first node during a condition window within a second phase of the clock input, wherein the condition window excludes at least a portion of the second phase, and wherein the second circuit is configured to conditionally generate the third state responsive to the condition signal during the condition window; and 3) a third circuit *(latch with Decoder output)* coupled to the first node and to the clock output, the third circuit configured to generate a third state on the clock output responsive to the first state

on the first node and configured to generate a fourth state on the clock output responsive to the second state on the first node.

With respect to claim 22, Weiss et al. discloses, in Fig. 6.7.2, that the second circuit is further configured to prevent charge sharing between the first node and a second node within the second circuit when the condition signal indicates that the second state is not to be generated on the clock output during the condition window.

With respect to claim 23, Weiss et al. discloses, in Fig. 6.7.2, that the second circuit comprises a first transistor coupled to the second node and having a first control node *(gate of 2nd N-transistor)* coupled to the condition signal, the first transistor charging the second node in response to the condition signal indicating that the second state is not to be generated on the clock output.

With respect to claim 24, Weiss et al. discloses, in Fig. 6.7.2, that the second circuit comprises a plurality of transistors coupled in series, wherein a first transistor of the plurality of transistors has a first control node *(gate of 1st transistor)* that is coupled to receive the clock input *(Half-frequency clock)* and a second transistor of the plurality of transistors has a second control node *(gate of 2nd transistor)* that is coupled to receive the condition signal *(from NOR gate)*, and wherein the second node is a node between the first transistor and the second transistor.

With respect to claim 25, Weiss et al. discloses, in Fig. 6.7.2, that the second circuit further comprises a third transistor coupled to the second node and having a third control node coupled to the condition signal, the third transistor charging the node in response to the condition signal indicating that the second state is not to be generated on the clock output.

With respect to claim 26, Weiss et al. discloses, in Fig. 6.7.2, that a third transistor having a third control node that is coupled to receive an inverse *(via the inverter)* of the clock input with a delay.

With respect to claim 27, Weiss et al. discloses, in Fig. 6.7.2, that the delay defines a width of the condition window.

With respect to claim 28, Weiss et al. discloses, in Fig. 6.7.2, the inverse of the clock input is generated by a logic gate coupled to receive the clock input and having an output coupled to the third control node.

With respect to claim 29, as best understood, Weiss et al. inherently discloses, in Fig. 6.7.2, that the logic gate is sized to generate the delay of ¼ of the second phase *(there would be a period created from the delay of the clock transitioning; this delay is greater than zero due to the two gates (gates of the inverter and n-transistor connected in series to the inverter) and is necessarily less than ½ of the second phase; this would be normally considered to be about ¼ delay of the second phase; therefore, this condition is met).*

With respect to claim 30, as best understood, Weiss et al. discloses, in Fig. 6.7.2, that the logic gate is sized to generate the delay of two gate delays *(gate of the inverter connected to the clock and gate of the N-transistor connected in series to the inverter).*

With respect to claim 31, Weiss et al. discloses, in Fig. 6.7.2, that the logic gate is an inverter.

With respect to claim 32, Weiss et al. discloses, in Fig. 6.7.2, that the third circuit comprises a latch circuit configured to hold the clock output during the portion of the second phase that is excluded from the condition window.

With respect to claim 33, as best understood, Weiss et al. inherently discloses, in Fig. 6.7.2, that the condition window is about ¼ of the second phase *(there would be a period created from the delay of the clock transitioning; this delay is greater than zero due to the two gates (gates of the inverter and n-transistor connected in series to the inverter) and is necessarily less than ½ of the second phase; this would be normally considered to be about ¼ delay of the second phase; therefore, this condition is met).*

With respect to claim 34, as best understood, Weiss et al. discloses, in Fig. 6.7.2, that the condition window is about two gate delays *(gate of the inverter connected to the clock and gate of the N-transistor connected in series to the inverter).*

With respect to claim 42, Weiss et al. discloses, in Fig. 6.7.2, a computer accessible medium *(page 112, col. 1, second paragraph, lines 3-7)* comprising a data structure representing (1) 1) a first circuit *(first P-transistor connected to clock)* coupled to receive the clock input and coupled to a first node within the conditional clock buffer circuit, the first circuit configured to generate a first state on the first node responsive to a first phase of the clock input; 2) a second circuit *including the three N transistors)* coupled to receive the clock input and the condition signal and coupled to the first node, wherein the second circuit is configured to conditionally generate a second state on the first node during a condition window within a second phase of the clock input, wherein the condition window excludes at least a portion of the second phase, and wherein the second circuit is configured to conditionally generate the third state responsive to the condition signal during the condition window; and 3) a third circuit *(latch with Decoder output)* coupled to the first node and to the clock output, the third circuit configured to generate a third

state on the clock output responsive to the first state on the first node and configured to generate a fourth state on the clock output responsive to the second state on the first node.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 35-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weiss et al. (IEEE International Solid-State Circuits Conference, ISSCC 2002, February 2002, pp 112-113) in view of Schmidt (U.S. Patent No. 5,838,179).

With respect to claim 35, Weiss et al. discloses, in Fig. 6.7.2, a conditional clock buffer circuit coupled to receive a buffered clock [Clock] and a condition signal [*output from NOR gate*]; the conditional clock buffer circuit having a clock output [Decoder output] and comprising (1) a first circuit *(first P-transistor connected to clock)* (i) coupled to receive the buffered clock [Clock], and (ii) configured to generate a first state on the clock output responsive to a first phase of the buffered clock, and (2) a second circuit *including the three N transistors)* coupled to receive the clock input and the condition signal and coupled to the first node, wherein the second circuit is configured to conditionally generate a second state on the first node during a condition window within a second phase of the clock input, wherein the condition window excludes at least a portion of the second phase, and wherein the second circuit is configured to conditionally generate the third state responsive to the condition signal during the condition window; and 3) a third circuit *(latch with Decoder output)* coupled to the first node and to the clock output, the

third circuit configured to generate a third state on the clock output responsive to the first state on the first node and configured to generate a fourth state on the clock output responsive to the second state on the first node. Weiss et al. fails to disclose a clock tree comprising one or more levels of buffering coupled to receive an input clock and output a buffered clock.

Schmidt discloses, in figure 1, a clock tree [12] comprising multiple levels of buffering coupled to receive an input clock [TRECLKIN] and output a buffered clock [TRECLK0,..., TRECLK8].

To implement the conditional clock buffer circuit of Weiss et al. by connecting it to the output of the clock tree taught by Schmidt to construct a clock distribution system necessary for a data structure network with efficient synchronization would have been deemed obvious to one of ordinary skill in the art at the time of the invention since Schmidt teaches that such a clock tree could be employed to minimize clock skew and clock loading for any given clock driver at the output *(see Schmidt; col. 1, lines 21-24; col. 3, lines 16-19).*

With respect to claim 36, Weiss et al. discloses, in Fig. 6.7.2, that the second circuit is further configured to prevent charge sharing between the first node and a second node within the second circuit when the condition signal indicates that the second state is not to be generated on the clock output during the condition window.

With respect to claim 37, Weiss et al. discloses, in Fig. 6.7.2, that the second circuit comprises a first transistor coupled to the second node and having a first control node *(gate of 2nd N-transistor)* coupled to the condition signal, the first transistor charging the second node in response to the condition signal indicating that the second state is not to be generated on the clock output.

With respect to claim 38, Weiss et al. discloses, in Fig. 6.7.2, that the second circuit comprises a plurality of transistors coupled in series, wherein a first transistor of the plurality of transistors has a first control node *(gate of 1st transistor)* that is coupled to receive the clock input *(Half-frequency clock)* and a second transistor of the plurality of transistors has a second control node *(gate of 2nd transistor)* that is coupled to receive the condition signal *(from NOR gate)*, and wherein the second node is a node between the first transistor and the second transistor.

With respect to claim 39, Weiss et al. discloses, in Fig. 6.7.2, that the third circuit comprises a latch circuit *(circuitry part connected to the output including 2 P-transistors and 2 N-transistors)* configured to hold the clock output during the portion of the second phase that is excluded from the condition window.

With respect to claim 40, as best understood, Weiss et al. inherently discloses, in Fig. 6.7.2, that the condition window is about ¼ of the second phase *(there would be a period created from the delay of the clock transitioning; this delay is greater than zero due to the two gates (gates of the inverter and n-transistor connected in series to the inverter) and is necessarily less than ½ of the second phase; this would be normally considered to be about ¼ delay of the second phase; therefore, this condition is met).*

With respect to claim 41, as best understood, Weiss et al. discloses, in Fig. 6.7.2, that the condition window is about two gate delays *(gate of the inverter connected to the clock and gate of the N-transistor connected in series to the inverter).*

Citation of Relevant Prior Art

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Lin (U.S. Patent No. 6,618,283) discloses a system and method for skew compensating a clock signal and for capturing a digital signal using the skew compensated clock signal.

Prior art Yoo et al. (U.S. Patent No. 6,625,242) delay locked loop and methods that shift the phase of a delayed clock signal based on a reference phase value.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (703) 305-0414. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703) 308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 305-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Linh M. Nguyen
Examiner
Art Unit 2816

LMN